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06EC46

Fourth Semester B.E. Degree Examination, Dec.2015/Jan.2016

Linear IC's and Applications

Time: 3 hrs. Max. Marks:100

Note: ***Answer FIVE full questions, selecting at least TWO questions from each part.***

PART – A

1 a. Define the following:
i) Differential amplifier ii) CMRR iii) Slew rate
iv) PSRR v) Input offset voltage and current **(10 Marks)**

b. With the help of neat diagram, design a direct coupled non-inverting amplifier to have a voltage gain of approximately 66. The signal amplitude is to be 15 mV.
Given: $I_{B(max)} = 600$ nA. **(10 Marks)**

2 a. Write short notes on:
i) Setting up the upper cutoff frequency for an inverting amplifier.
ii) Use of single polarity supply in voltage follower. **(10 Marks)**

b. Design a capacitor coupled non-inverting amplifier using 741 op-amp, with the following specification:
i) With a +24V supply
ii) Voltage gain of 100
iii) Output amplitude of 5V
iv) Lower cut-off frequency of 75 Hz
v) $R_{L(min)} = 5.6$ KΩ. **(10 Marks)**

3 a. Define: i) loop gain, ii) loop phase shift, iii) unity gain BW. **(06 Marks)**

b. What is frequency compensation? Explain phone lag compensation network. **(06 Marks)**

c. Calculate the slew rate-limited cutoff frequency for a voltage follower circuit using 741 op-amp if the peak of sine wave output is to be 5 V.
i) Determine maximum peak value of sinusoidal output voltage that will allow the 741 voltage follower CFT to operate at 800 kHz unity-gain cut off frequency.
ii) Calculate maximum peak value of sine wave output voltage that can be produced by the amplifier if frequency is 8 kHz. Given slew rate S = 0.5 V/μs. **(08 Marks)**

4 a. With the help of neat diagram, explain Zener diode peak clipper. **(08 Marks)**

b. With the help of neat CFT diagram, design an instrumentation amplifier to have an overall voltage gain of 900. The input signal amplitude is 15 mV, 741 op-amps are to be used and supply is ±15 V. Assume $I_2 = 50$ μA and I5 (100 I_{Bmax}) **(12 Marks)**

PART – B

5 a. With the help of neat circuit diagram, explain the working of sample and hold circuit. **(08 Marks)**

b. Derive, $V_{0_{comp}} = \left(1+\frac{R_2}{R_{TC}}\right)\frac{KT}{q}\ell n\left(\frac{vi}{V_{ref}}\right)$ for an log amplifier, where R_2 = feedback resistance of last op-amp stage R_{TC} = temperature sensitive resistance with positive co-efficient of temperature. **(12 Marks)**

6 a. Draw the circuit diagram of an inverting Schmitt trigger using op-amp with UTP and LTP = ±xv > 0v. Draw the output, input waveforms. Explain clearly the operations. **(06 Marks)**

b. Design an astable multivibrator to have a ±av output with a frequency of 1 kHz. |UTP| = |LTP| = 0.5 V.

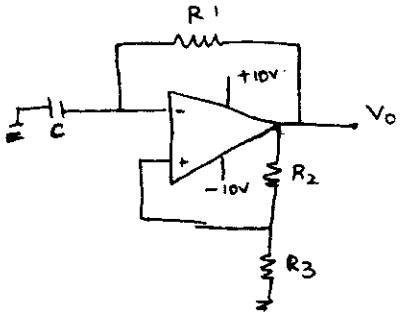

Fig.Q6(b) **(09 Marks)**

c. Design a first-order active low pass filter to have a cut off frequency of 1 kHz using μA 741 op-amp. $I_{B(max)}$ = 500 nA. **(05 Marks)**

7 a. Sketch the circuit of a regulated power supply and explain its operation. **(08 Marks)**

b. List and briefly explain the characteristics of 3 terminal IC regulators. What are the limitations of these regulators? **(07 Marks)**

c. Define and explain the following terms with respect to voltage regulator:
   i) Line regulation
   ii) Load regulation **(05 Marks)**

8 a. A 555 astable multivibrator has R_A = 2.2 KΩ, R_B = 3.9 KΩ, C = 0.1 μF. Calculate:
   i) t_{high}
   ii) t_{low}
   iii) free running frequency f_0 and % duty cycle
   Draw the circuit diagram. **(07 Marks)**

b. Explain the following for a PLL:
   i) Lock in range
   ii) Capture range
   iii) Pull in time **(06 Marks)**

c. With the help of neat diagram, explain the operation of R-2R ladder DAC. **(07 Marks)**

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